LINEAR FEEDBACK SHIFT REGISTER RESEEDING

Abstract

An apparatus has an integrated circuit that includes a seed register, a linear feedback shift register to load a test vector into a number of scan chains, and a signature register to receive a test response from the scan chains. The seed register, the linear feedback shift register, and the signature register each have the same register length. The linear feedback shift register and the signature register have the same shift frequency that is greater than a frequency at which a seed vector is loaded into the seed register. The linear feedback shift register is adapted to be selectively provided with bits to control a degree to which its vector is dependent on previous vectors. The scan chains may be configured as a single group providing a test response to a single input signature register or a set of groups providing a test response to a multiple input signature register.